(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 September 2005 (09.09.2005)

PCT

(10) International Publication Number
WO 2005/081976 A3

(51) International Patent Classification:
H01L 31/0256 (2006.01) *H01L 29/00* (2006.01)
H01L 31/0312 (2006.01) *H01L 23/48* (2006.01)

(21) International Application Number:
PCT/US2005/005749

(22) International Filing Date:
22 February 2005 (22.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/784,903 20 February 2004 (20.02.2004) US

(71) Applicant *(for all designated States except US)*: **ACTEL CORPORATION** [US/US]; 2061 Stierlin Court, Mountain View, CA 94043-4655 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **ISSAQ, A., Farid** [US/US]; 1217 Capri Drive, Campbell, CA 95008 (US). **HAWLEY, Frank**; 1360 Capri Drive, Campbell, CA 95008 (US). **MCCOLLUM, John** [US/US]; 19180 Merribrook Drive, Saratoga, CA 95070 (US).

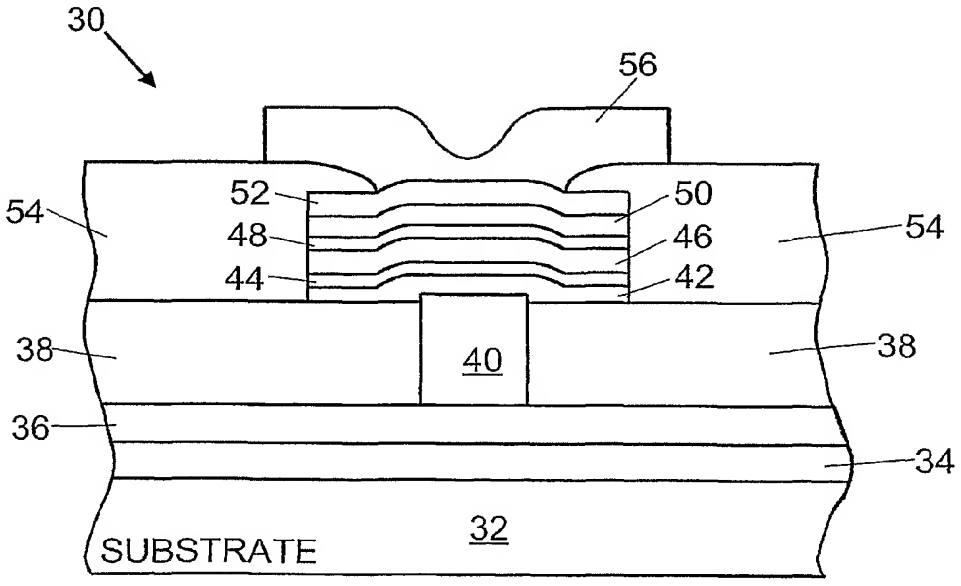
(74) Agent: **D'ALESSANDRO, Kenneth**; Sierra Patent Group, Ltd., P.O. Box 6149, Stateline, NV 89449 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,

[Continued on next page]

(54) Title: REPROGRAMMABLE METAL-TO-METAL ANTIFUSE EMPLOYING CARBON-CONTAINING ANTIFUSE MATERIAL



(57) Abstract: A reprogrammable metal-to-metal antifuse is disposed between two metal interconnect layers in an integrated circuit. A lower barrier layer is formed from Ti. A lower adhesion-promoting layer is disposed over the lower Ti barrier layer. An antifuse material layer selected from a group comprising at least one of amorphous carbon and amorphous carbon doped with at least one of hydrogen and fluorine is disposed over the lower adhesion-promoting layer. An upper adhesion-promoting layer is disposed over the antifuse material layer. An upper Ti barrier layer is disposed over the upper adhesion-promoting layer.

WO 2005/081976 A3

SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
12 January 2006

(48) Date of publication of this corrected version:
24 August 2006

(15) Information about Correction:
see PCT Gazette No. 34/2006 of 24 August 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

REPROGRAMMABLE METAL-TO-METAL ANTIFUSE EMPLOYING CARBON-CONTAINING ANTIFUSE MATERIAL

BACKGROUND

1. Field Of The Invention

The present invention relates to amorphous carbon metal-to-metal antifuse structures. More particularly, the present invention relates to reprogrammable amorphous carbon metal-to-metal antifuse structures employing adhesion layers and titanium (Ti) barrier layers.

2. The Background Art

Integrated electronic circuits are typically fabricated with all internal connections set during the manufacturing process. However, because of high development costs and high manufacturing tooling costs of such circuits, it is advantageous for integrated circuits to be configured or programmed by the user to implement a desired application. Such circuits are called programmable circuits, and antifuses are known in the art for providing the programmability of these circuits. Antifuses are devices that generally comprise a pair of conductive electrodes sandwiched about an insulating antifuse material layer.

A programming process disrupts the antifuse material and forms a filament between the two electrodes. Prior to programming, antifuses exhibit a resistance as high as a few gigaohms between the two electrodes and may be considered to be open circuits. The programming process creates a low-impedance connection of a few ohms to a few thousand ohms between the two electrodes. Programming voltages range from a few volts to about 20 volts.

It is known in the art that antifuses have been fabricated where the electrodes have been selected from a number of different electrically conductive layer materials, and the antifuse material layer has been fabricated from a number of different insulating materials. It is also known that many different antifuse structures have been proposed, including, "via" type, half-stacks, full stacks, conductive plugs and numerous other variations.

Antifuses are generally classified into two categories. A first type of antifuse, referred to as a substrate antifuse, has a doped region in a semiconductor substrate as its lower electrode and a layer of metal or doped polysilicon as its upper electrode. The antifuse

material typically comprises one or more layers of silicon nitride or silicon dioxide. An example of such an antifuse is made of an oxide-nitride-oxide (ONO) antifuse material layer sandwiched between an N+ diffusion layer and a polysilicon ("Poly") layer (N+/ONO/Poly). Such a device is described in detail in United States Patents Nos. 4,823,181 and 4,881,114. For this category of antifuse, contacts have to be made to the N+ diffusion layer and the upper electrode from two corresponding conductive metal lines.

There are known problems with substrate-level antifuses. Some of the suggested dielectric materials require complex manufacturing techniques and have low reliability during programming. Some programmed antifuses may have a finite resistance on the order of several hundred to several thousand ohms which may render them relatively unsuitable for use in high speed circuits, and also result in high power consumption when a large number of circuits are switching simultaneously. Further, to maintain reliable operation at commercially acceptable voltages, proposed antifuse material layers are typically thin enough to produce a relatively high capacitance. This can place a limit on device operating speed because antifuses on a single line act as capacitors linked in parallel, such that the sum of the individual capacitances of the unprogrammed antifuses can slow data signals undesirably. Finally, substrate antifuses consume a lot of chip area.

A second type of antifuse, referred to as a metal-to-metal antifuse has a first metal layer disposed above and insulated from a semiconductor substrate as its lower electrode, a second metal layer as its upper electrode, and an antifuse material layer sandwiched between the first and second layers of metal. The antifuse material layer may be accompanied by one or more barrier metal layers separating it from lower and upper metal interconnect layers. Numerous structures for metal-to-metal antifuses are known in the art. Illustrative and non-exhaustive examples of metal-to-metal antifuses are shown in United States Patent No. 5,272,101 to Forouhi et al.

The resistance of a programmed metal-to-metal antifuse is typically much lower than a programmed substrate level antifuse. During programming of a metal-to-metal antifuse, the metallization layers in the vicinity of the antifuse, the antifuse material layer and a portion of the adjacent metallization layers will disrupt and/or melt, and a conductive link will form through the antifuse material layer due to metal from the adjacent metallization layer being drawn in and intermixed through mass transport and thermal driven material diffusion and chemical reaction which is specific for an a-Silicon metal-to-metal antifuse.

Metal-to-metal antifuses usually employ a layer of amorphous silicon as the antifuse material, however, they may also employ oxide and nitride layers either alone or in multilayer combinations, or in combinations with amorphous silicon. Examples of antifuses that have been suggested using one or more oxide or nitride layers as antifuse material layers include United States Patent No. 4,543,594 to Mohsen et al., United States Patent No. 4,823,181 to Mohsen et al., United States Patent No. 4,899,205 to Hamdy et al. Examples of antifuses that have been suggested using amorphous silicon as an antifuse material layer, either by itself, or in combination with one or more oxide or nitride layers include United States Patent No. 5,070,384 to McCollum et al., United States Patent No. 5,171,715 to Husher et al., and United States Patent No. 5,181,096 to Forouhi et al., United States Patent No. 5,272,101 to Forouhi et al., and United States Patent No. 5,196,724 to Gordon.

Antifuse capacitance, as described above, is also a problem for metal-to-metal antifuses. Amorphous silicon antifuses alleviate this problem by providing a relatively thick antifuse layer, however, amorphous silicon antifuses exhibit relatively high leakage currents. Another approach has been to form a leakage barrier between the electrodes and the amorphous silicon antifuse material. A thin layer of deposited silicon dioxide or silicon nitride has been used. If this layer is too thin, it will not be an effective barrier, and if it is too thick, it will appreciably raise the programming voltage of the antifuse.

It is known that a-Silicon metal-to-metal antifuses will exhibit, under specific conditions where excessive current is placed across a programmed antifuse, a phenomenon wherein the conductive links will open up or become non-conductive. This failure mode is commonly known as "read disturb" because an excessive parasitic current occurs during the read state of the antifuse.

One factor that contributes to read disturb is the presence of any significant quantity of aluminum in the antifuse conductive links due to electromigration of the aluminum. Metal Barrier layers which serve to block aluminum flow into the antifuse material layer of various materials and various thicknesses have been proposed. The barrier materials, between the aluminum and the amorphous silicon, provide essentially all of the conductive material forming the conductive filament in the programmed antifuse. An antifuse formed with such a barrier metal link material can tolerate more current and have a higher reliability than an antifuse formed without the barrier metal link material.

Another way to overcome this problem is to change the composition of the antifuse material. For example, an amorphous silicon antifuse layer may be replaced with another low-temperature dielectric, such as oxide, nitride, or combinations of oxide and nitride have lower leakage current and higher breakdown voltage. Therefore, to maintain the same breakdown voltage requirements, the thickness of the antifuse dielectric has to be reduced. However, reducing the thickness of the antifuse material layer results in an increase in the capacitance of the antifuse in its unprogrammed state. This increased capacitance has a negative impact on the product speed.

Other materials which are harder and denser than amorphous silicon, such as silicon carbide (SiC) and amorphous carbon have been proposed to replace amorphous silicon to reduce the read disturb phenomenon and other problems associated with amorphous silicon metal-to-metal antifuses. It is important to employ these materials at desired programming voltages, and with a minimum of capacitance.

Amorphous carbon has been shown to significantly address the read disturb phenomenon. One problem in employing amorphous carbon as the antifuse material layer has been that it can fail to adhere to a metal electrode. Adhesion of the layers in a thin film device typically occurs because there is either ionic bonding at the interface of the films, metallurgical bonding where a chemical reaction between the materials results in a new material, or mechanical adhesion where the adhesion is due to the deposited film hooking onto surface nooks and projections.

When materials in a thin film device do not adhere to one another, a "glue" layer must be employed. In an amorphous-carbon based antifuse device, the problem of finding a glue layer material is difficult because a suitable glue layer material must adhere to both the metal electrode and the amorphous-carbon antifuse material layer. Concurrently, the adhesion material of the glue layer employed should have minimal impact on the programming and capacitance characteristics of the antifuse.

One other characteristic that is common to prior-art antifuses is that they have typically been only one-time programmable, that is that the programming mechanism that creates the low-resistance connection between the two antifuse electrodes has been irreversible. Once the antifuse has been programmed it becomes a permanent low-resistance connection. Controllable reprogramming of antifuses has been an elusive goal.

SUMMARY

A reprogrammable metal-to-metal antifuse is disposed between two metal interconnect layers in an integrated circuit. A lower barrier layer is formed from Ti. A lower adhesion-promoting layer is disposed over the lower Ti barrier layer. An antifuse material layer selected from a group comprising at least one of amorphous carbon and amorphous carbon doped with at least one of hydrogen and fluorine is disposed over the lower adhesion-promoting layer. An upper adhesion-promoting layer is disposed over the antifuse material layer. An upper Ti barrier layer is disposed over the upper adhesion-promoting layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates schematically in a cross-sectional view a reprogrammable metal-to-metal antifuse according to the present invention.

FIG. 2A illustrates in a cross-sectional view a first embodiment of a reprogrammable metal-to-metal antifuse structure employing the tri-layer thin adhesion layer/a-C/thin adhesion layer structure according to the present invention.

FIG. 2B illustrates in a cross-sectional view a second embodiment of a reprogrammable metal-to-metal antifuse structure employing the tri-layer thin adhesion layer/a-C/thin adhesion layer structure according to the present invention.

FIGS. 3A through 3E are cross-sectional views of the reprogrammable metal-to-metal antifuses of FIGS. 2A and 2B showing the structures existing at selected points in the fabrication process according to the present invention.

FIG. 4 is a set of IV curves showing three cycles of programming and erasing of an antifuse according to the present invention.

FIG. 5 is a block diagram illustrating a typical program/erase cycle that can be used with the reprogrammable antifuse of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

In FIG. 1, a reprogrammable antifuse 10 according to the present invention is depicted generally in a cross-sectional view. The reprogrammable antifuse 10 is disposed

between a lower metal interconnect layer 12 and an upper metal interconnect layer 14. Lower metal interconnect layer 12 and upper metal interconnect layer 14 are disposed above a semiconductor substrate 16 and an intervening insulating layer 18. The antifuse 10 has a lower Ti barrier layer 20, a lower adhesion-promoting layer 22 comprised of a material selected from the group comprising Si_xC_y and Si_xN_y, an antifuse material layer 24 formed from amorphous carbon or amorphous carbon doped with at least one of hydrogen and fluorine, an upper adhesion-promoting layer 26 comprised of a material selected from the group comprising Si_xC_y and Si_xN_y, and an upper Ti barrier layer 28. The lower and upper adhesion-promoting layers 22 and 26, respectively, are employed to provide adhesion between the antifuse material layer 20 and the lower and upper Ti barrier 20 and 28, respectively.

According to the present invention, the adhesion-promoting layers 22 and 26 should minimize the capacitance and do little to degrade the switching performance of the antifuse 10. The material for the adhesion-promoting layers 22 and 26 is preferably silicon carbide (Si_xC_y) where the ratio of x to y is 1.0 +/- 0.4. Depending on the ratio of x to y, the dielectric constant of the SiC layer will be the range of about 4 to about 6. The adhesion-promoting layers 22 and 26 should not substantially affect the electrical characteristics of antifuse 10 controlled by the antifuse material layer 24, such that the breakdown voltage, capacitance or leakage of the antifuse may not change by more than about ten percent, and are preferably quite thin.

As such, the adhesion-promoting layers 22 and 26 may be between one and a few atoms thick giving a thickness for the adhesion-promoting layers 22 and 26 a range of about 2 angstroms to about 20 angstroms. It should be appreciated that a layer having a thickness of 2 angstroms represents an average material layer thickness. For example, in a sparsely dense atomic monolayer there may be sufficient space between the individual atoms of the monolayer that a measured thickness will give an average thickness of the sparsely spaced atoms. The Si_xC_y may be deposited using PECVD techniques that are well known to those of ordinary skill in the art.

In determining the capacitance of the antifuse 10, the capacitance of the structure, which includes adhesion-promoting layer 22, antifuse material layer 24, and adhesion-promoting layer 26, is the total series capacitance of layers 22, 24 and 26. A structure including a 2 angstrom layer of Si_xC_y, a 100 angstrom layer of amorphous carbon having a

dielectric constant of about 2.5 to about 4, and a 2 angstrom layer of Si_xC_y, will have a dielectric constant of about 4, and a structure including a 20 angstrom layer of Si_xC_y, a 100 angstrom layer of amorphous carbon, and a 20 angstrom layer of Si_xC_y will have a dielectric constant of about 5.5.

Silicon nitride (Si_xN_y) where the ratio of x to y is about 0.75 +/- 0.225 may also be employed as the adhesion-promoting layers 22 and 26 according to the present invention. The Si_xN_y may be deposited using PECVD techniques well known to those of ordinary skill in the art. The dielectric constant of the Si_xN_y layer will be in the range of about 6 to about 8, so that the dielectric constant for a tri-layer structure of Si_xN_y /amorphous carbon/ Si_xN_y with material layer thicknesses comparable to the material layer thicknesses of the tri-layer structure of Si_xC_y/amorphous carbon/ Si_xC_y described above will be higher than the dielectric constant for the Si_xC_y /amorphous carbon/ Si_xC_y tri-layer structure.

Silicon Carbide Nitride ($Si_xC_yN_z$) where the ratio of x to y to z is (1:1:1) +/- 0.40 for any ratio may also be employed as the adhesion-promoting layers 22 and 26 according to the present invention. The SiCN may be deposited using PECVD techniques well known to those of ordinary skill in the art. The dielectric constant of the SiCN layer will be in the range of about 4 to about 8, so that the dielectric constant for a SiCN/amorphous carbon/SiCN structure with material layer thicknesses comparable to the material layer thicknesses of the SiC/amorphous carbon/ Si_xC_y structure described above will be higher than the dielectric constant for the Si_xC_y /amorphous carbon/ Si_xC_y structure.

The antifuse material layer 24 may be formed from amorphous carbon or amorphous carbon doped with hydrogen and/or fluorine. The thickness of antifuse material layer 24 has a range of about 50 angstroms to about 500 angstroms for a breakdown voltage of about 3V to about 20V. Preferably, the thickness of the antifuse material layer 24 is about 100 angstroms for breakdown of 5 volts. When the antifuse material layer 24 is formed from amorphous carbon doped with hydrogen, the hydrogen doping should be from about 1 atomic percent to about 40 atomic percent. The amorphous carbon, and combinations thereof, may be disposed by a source gas, preferably acetylene gas (C_2H_2).

FIGS. 2A and 2B illustrates in cross-section a metal-plug embodiment of a reprogrammable metal-to-metal antifuse structure 30 according to the present invention. In the embodiment shown in FIGS. 2A and 2B, substrate 32 is covered by an insulating layer 34 and a metal interconnect layer 36. Persons of ordinary skill in the art will realize FIGS.

2A and 2B are merely illustrative and that metal interconnect layer 36 is not necessarily the first metal interconnect layer in a multi-level integrated circuit.

Insulating layer 38, formed from, for example, deposited silicon dioxide having a thickness from between about 400 nanometers (nm) to about 1000 nm, is disposed above metal interconnect layer 36 and includes a tungsten (W) plug 40 formed in a via therethrough and electrically coupled to metal interconnect layer 36. As is known in the art, the upper surfaces of insulating layer 38 and W plug 40 may be planarized to provide a relatively flat surface upon which to fabricate antifuse 30. Alternatively, W plug 40 may be raised above the surface of the surface of the insulating layer 38 as shown diagramatically in FIG. 2A and 2B by performing planarization using techniques such aschemical/mechanical polishing (CMP) or by performing a plasma oxide etch after planarization.

W plug 40 forms the lower electrode of antifuse 30. As depicted in FIGS. 2A and 2B, a Ti barrier metal layer 42 having a thickness of about 25 nm to about 200 nm is disposed over the W plug 40.

According to the present invention, a thin lower adhesion-promoting layer 44 formed from either Si_xC_y, Si_xN_y, or SiCN having a thickness of about 2 angstroms to about 20 angstroms, or other suitable adhesion-promoting layer, as described above, is disposed over the lower Ti barrier metal layer 42 lying on the tungsten plug 40. An antifuse material layer 46 of amorphous carbon or amorphous carbon doped with hydrogen and having a thickness of about 2.5 nm to about 1000 nm is disposed over the lower adhesion-promoting layer 44. A thin upper adhesion-promoting layer 48 formed from either Si_xC_y, Si_xN_y, SiCN having a thickness of about 2 angstroms to about 20 angstroms, or other suitable adhesion-promoting layer, as described above, is disposed over antifuse material layer 44.

A Ti barrier metal layer 50 forming an upper antifuse electrode having a thickness of about 25 nm to about 200 nm is disposed over the adhesion-promoting layer 48. A hard mask layer 52 is deposited over barrier metal layer 48. In FIG. 2B, the hardmask layer is formed form an insulating material such as silicon dioxide, and in FIG. 2A, the hardmask layer is formed from W.

In both FIGS. 2A and 2B, an insulating layer 54 of deposited silicon dioxide having a thickness of about 100 nm to about 200 nm is formed over the structure including lower adhesion-promoting layer 44, antifuse material layer 46, upper adhesion-promoting layer 48, and barrier metal layer 50. In FIG. 2B, metal interconnect layer 56 is disposed over the

insulating layer 54 and contacts barrier metal layer 50 by a via formed through hardmask oxide layer 52 and insulating layer 54. In FIG. 2A, metal interconnect layer 56 is disposed over the insulating layer 54 and contacts the upper surface of W hardmask layer 52 by a via formed through insulating layer 54. As will be appreciated by persons of ordinary skill in the art, no etching step through hardmask layer 52 is necessary in the embodiment shown in FIG. 2A since the hardmask layer is formed from a conducting material.

The hardmask layer 52 is patterned and etched to form a hardmask that will act as an etch mask when etching barrier metal layer 50, upper adhesion-promoting layer 48, antifuse material layer 46, and lower adhesion-promoting layer 44 to form an antifuse "stack". Such a mask is used instead of a photoresist mask, since a subsequent photoresist-removal step would necessarily employ an etchant effective on organic materials. Such etchants would attack the exposed side edges of the carbon antifuse material layer 46.

When silicon dioxide is employed as hardmask layer 52, it protects the antifuse material layer 46 from being removed during a photoresist stripping step. Alternatively, Since Ti has high selectivity to W, a thin layer of PVD W in a range of about 25 nm to about 50 nm can also be employed as the hardmask layer 52 to etch the barrier metal layer 48. The oxide or W hardmask provides high etch selectivity and ability to etch metals without affecting the dielectric constant and the mechanical properties of the amorphous carbon antifuse material layer 44.

FIGS. 3A through 3E are cross-sectional views of the antifuses of FIGS. 2A and 2B showing the structure existing at selected points in the fabrication process. Since the fabrication of antifuse 30 begins after the well-known prior processing steps used to planarize insulating layer 38 and W plug 4, FIG. 3A shows the planarized insulating layer 38 and W plug 40 as the starting point for the fabrication process.

As may be seen from an examination of FIG. 3A, antifuse 30 of FIGS. 2A and 2B is fabricated by forming a lower Ti barrier layer 42 over the insulating layer 38 and the exposed top of W plug 40. Next, adhesion-promoting layer 44 is formed over Ti barrier layer 42. The adhesion-promoting layer 44 should be quite thin to minimize the effects on electrical characteristics of the antifuse material layer 46. As such, the adhesion-promoting layer 44 may be between one and a few atoms thick, i.e., in the range of between about 2 angstroms to about 20 angstroms. When either Si_xC_y, Si_xN_y, or $Si_xC_yN_z$ are employed as adhesion-promoting layer 44, either of the Si_xC_y, Si_xN_y, or $Si_xC_yN_z$ may be deposited using

PECVD techniques well known to those of ordinary skill in the art.

Next, an antifuse material layer 46 formed from amorphous carbon or hydrogen-doped amorphous carbon is then deposited on adhesion-promoting layer 44 to a thickness in the range of between about 50 angstroms to about 500 angstroms using PECVD techniques well known to those of ordinary skill in the art. It will be appreciated by those of ordinary skill in the art that the thickness of the antifuse material layer employed will depend on the desired programming voltage for the finished antifuse 30.

Next, an upper adhesion-promoting layer 48 is deposited over amorphous carbon antifuse material layer 46. The adhesion-promoting layer 48 should be quite thin to minimize the effects on the electrical characteristics of the antifuse material layer 46. As such, the adhesion-promoting layer 48 may be between one and a few atoms thick, i.e., in the range of between about 2 angstroms to about 20 angstroms. When either Si_xC_y, Si_xN_y, SiCN are employed as adhesion-promoting layer 48, either the Si_xC_y, Si_xN_y, SiCN are deposited using PECVD techniques well known to those of ordinary skill in the art.

Next, Ti barrier layer 50 is deposited to a thickness of between about 25 nm to about 200 nm using PVD sputtering techniques well known to those of ordinary skill in the art. Hardmask layer 52 is then deposited over barrier metal layer 50. When the hardmask layer 52 is formed from an insulating material such as silicon dioxide, it may be deposited to a thickness between about 50 nm and about 400 nm, with about 200 nm preferred, using, for example, PECVD techniques well known to those of ordinary skill in the art. When the hardmask layer 52 is formed from W, it may be deposited to a thickness of between about 25 nm and about 50 nm using PVD sputtering techniques well known to those of ordinary skill in the art. FIG. 3A shows the structure resulting after these processing steps have been performed.

Referring now to FIG. 3B, a photoresist layer 60 is deposited and patterned on the hardmask layer 52, using conventional photolithography steps. Hardmask 52 is then etched using conventional processing techniques appropriate to its composition. FIG. 3B shows the structure resulting after these processing steps have been performed.

Referring now to FIG. 3C, the photoresist layer 60 is then stripped exposing the remaining patterned hardmask layer 52. The patterned hardmask layer 52 is left to act as an etch mask when etching lower Ti barrier layer 42, lower adhesion-promoting layer 44, antifuse material layer 46, upper adhesion-promoting layer 48, and upper Ti barrier layer 50

to form the antifuse stack. The antifuse stack is then etched using conventional processing techniques. FIG. 3C shows the structure resulting after these processing steps have been performed.

In FIGS. 3D and 3E, an insulating layer 54 of silicon dioxide having a thickness of about 100 nm to about 200 nm is deposited using, for example, PECVD techniques well known to those of ordinary skill in the art over the structure including lower adhesion-promoting layer 42, antifuse material layer 44, upper adhesion-promoting layer 46, barrier metal layer 48, and hardmask layer 50. In FIG. 3E, metal interconnect layer 56 is disposed over the insulating layer 54 and contacts barrier metal layer 50 by a via formed through hardmask oxide layer 52 and insulating layer 54. In FIG. 3D, metal interconnect layer 56 is disposed over the insulating layer 54 and contacts hardmask W layer 52 by a via formed through insulating layer 54. The metal interconnect layer 56 may be formed using PVD sputtering. The vias are formed in FIGS. 3E and 3F using conventional processing techniques.

The adhesion-promoting layers should minimize the capacitance of and do little to degrade the switching performance of the antifuse. The adhesion-promoting layers may be quite thin in a range of between about 2 angstroms and about 20 angstroms to minimize the effects on electrical characteristics of the antifuse material layer. The material for the adhesion-promoting layers is preferably silicon carbide (Si_xC_y). Depending on the ratio of x to y, the dielectric constant of the Si_xC_y layer will be the range of between about 4 and about 6. Silicon nitride (Si_xN_y) may also be employed as the adhesion-promoting layers according to the present invention. Depending on the ratio of x to y, the dielectric constant of the Si_xN_y layer will be the range of about 6 to about 8. Silicon Carbide Nitride ($Si_xC_yN_z$) where the ratio of x to y to z is about (1:1:1) +/- 0.40 for any ratio may also be employed as the adhesion-promoting layers. The dielectric constant of the $Si_xC_yN_z$ layer will be in the range of between about 4 and about 8. The adhesion-promoting layers are deposited using PECVD techniques well known to those of ordinary skill in the art.

For an antifuse material layer of amorphous carbon having a dielectric constant of about 2.5 to about 4, a tri-layer structure including a 2 angstrom layer of Si_xC_y, a 100 angstrom layer of amorphous carbon, and a 2 angstrom layer of Si_xC_y, will have a dielectric constant of about 4, and a tri-layer structure including a 20 angstrom layer of Si_xC_y, a 100 angstrom layer of amorphous carbon, and a 20 angstrom layer of Si_xC_y, will have a dielectric

constant of about 5.5. The dielectric constant for a tri-layer structure of Si_xN_y /amorphous carbon/ Si_xN_y with material layer thicknesses comparable to the material layer thicknesses of the tri-layer structure of Si_xC_y /amorphous carbon/ Si_xC_y will be higher than the dielectric constant for the Si_xC_y /amorphous carbon/ Si_xC_y tri-layer structure.

The antifuse according to the present invention is reprogrammable according to the method of the present invention. It may be programmed, and erased and reprogrammed. As is known in the art, antifuses are programmed by applying a programming potential across them until a sharp rise in current flow is sensed, indicating that a low-resistance connection has been established between the electrodes. As with prior-art antifuses, one or more "soak" cycles may be performed on the antifuse after programming as is known in the art.

The antifuse according to this invention can be programmed at low current of between 100uA to 1mA. The link formed at low current has low resistance (below 500 ohm). The subsequent soaking of the antifuse link, with a higher current up to 5mA reduces the resistance further and tightens the programmed-resistance distribution.

The antifuse programmed at low current i.e. less than about 1mA can be erased to the original off state condition (high resistance state) when subjected to a high current relative to the programming current i.e. about 10mA to about 15mA, a ratio of about 10:1 programming to erase current. Another case is when the link is formed with a programming current of less than about 1mA and soaked with less than about 5mA. This case will have a higher erase current i.e. about 15mA to about 20mA, a ratio of greater than about 3:1 soak to erase current.

The high ratio of switching current (erase current) to programming current indicates a reliable antifuse. The antifuse programmed and erased can be reprogrammed at voltages similar to the original programming voltages. In addition, the erased antifuse will have similar but somewhat higher leakage characteristics as compared to the original.

FIG. 4 is a set of IV curves showing three cycles of programming and erasing of an antifuse according to the present invention. The curves of FIG. 4 were plotted for an antifuse with an amorphous carbon antifuse layer as disclosed herein having a thickness of about 300 angstroms. As may be seen from an examination of FIG. 4, the antifuse programmed at voltages between about 8.2 to about 8.5 volts over the three programming cycles that were performed. Persons of ordinary skill in the art will appreciate that the programming voltage for an antifuse fabricated according to the present invention will be a function of the

thickness of the amorphous carbon antifuse material layer.

After the antifuse is programmed, the circuit in which it is contained may be operated at voltages significantly below the programming voltage. For the antifuse having the program and erase characteristics shown in FIG. 4, the maximum operating voltage should be about 0.75-2.5v.

As also shown in FIG. 4, the antifuse of the present invention may be erased (returned to a high-resistance state) by placing a voltage potential across it. It has been found that the erase voltage is much lower than the programming voltage. In the case of the antifuse having the characteristics shown in FIG. 4, the erase potential has been found to be between about 3.4 to about 3.6 volts and the erase current less than about 20 mA over the three programming cycles that were performed. With the absence of a resistor at probe tip (normal routine) the erase voltage will be less than about 1v. The explanation of the applied voltage is: the voltage is dependent on the circuit resistance, where the voltage is supplied to apply the erase current necessary to erase the antifuse. The example shown has a 250 ohm resistor at the probe tip of the device under test, this resistor is for preventing current dumping which may occur from the test setup equipment. Thus the applied voltage shown in this example is an artifact of the resistor in series, and not the critical parameter. The applied current is the critical parameter.

Referring now to FIG. 5, a block diagram illustrates a typical program/erase cycle that can be used with the reprogrammable antifuse of the present invention. First, as shown at reference numeral 60, the antifuse is subjected to a programming cycle as disclosed herein. Next, at reference numeral 62, the antifuse may be subjected to an erase cycle as disclosed herein. Because the reprogrammable antifuse of the present invention may not be reprogrammed an infinite number of times, the antifuse may then be checked at reference numeral 64 to see if the erase cycle has been successful, i.e., whether the antifuse has been returned to a high-resistance state. If the antifuse has been successfully returned to a high-resistance state, it may again be programmed as shown at reference numeral 66. If the antifuse has not been successfully returned to a high-resistance state, this indicates that it may not be erased and thus cannot again be programmed as shown at reference numeral 68. As will be appreciated by persons of ordinary skill in the art, the processes of reference numerals 60 through 68 may, but need not be, performed at times proximate to one another.

While the invention has been described with reference to an exemplary embodiment,

it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. For example, it is to be understood that oxygen may be included in the mixture of any materials disclosed for the adhesion-promoting layers, for example, in addition to Si_xC_y and Si_xN_y; $Si_xO_yC_z$ and $Si_xO_yN_z$ may be used, as well as similar mixtures of the other materials disclosed. In addition, many modifications may be made to adapt a particular situation or material to the teachings without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A reprogrammable metal-to-metal antifuse comprising:

a lower Ti barrier layer;

a lower adhesion-promoting layer disposed over said lower Ti barrier layer;

an antifuse material layer disposed above an upper surface of said lower adhesion-promoting layer lower Ti barrier layer, said antifuse material layer selected from a group comprising at least one of amorphous carbon and amorphous carbon doped with at least one of hydrogen and fluorine disposed over said lower adhesion-promoting layer;

an upper adhesion-promoting layer disposed over said antifuse material layer; and

an upper Ti barrier layer disposed over said upper adhesion-promoting layer.

2. The reprogrammable metal-to-metal antifuse of claim 1, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer each have a thickness of between about 2 angstroms and about 20 angstroms.

3. The reprogrammable metal-to-metal antifuse of claim 1, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer are comprised of a material selected from the group comprising Si_xC_y and Si_xN_y.

4. The reprogrammable metal-to-metal antifuse of claim 3, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xC_y.

5. The reprogrammable metal-to-metal antifuse of claim 4, wherein a ratio of x to y in said Si_xC_y is in a range of about 1 +/- 0.4.

6. The reprogrammable metal-to-metal antifuse of claim 3, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xN_y.

7. The reprogrammable metal-to-metal antifuse of claim 6, wherein a ratio of x to y in said Si_xN_y is in a range of about .75 +/- 0.225.

8. The reprogrammable metal-to-metal antifuse of claim 2, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer are from a material selected from the group comprising Si_xC_y and Si_xN_y.

9. The reprogrammable metal-to-metal antifuse of claim 8, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xC_y.

10. The reprogrammable metal-to-metal antifuse of claim 9, wherein a ratio of x to y in said Si_xC_y is in a range of about 1 +/- 0.4.

11. The reprogrammable metal-to-metal antifuse of claim 8, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xN_y.

12. The reprogrammable metal-to-metal antifuse of claim 8, wherein a ratio of x to y in said Si_xN_y is in a range of about .75 +/- 0.225.

13. The reprogrammable metal-to-metal antifuse of claim 1, wherein said antifuse material layer is formed from amorphous carbon having a thickness of between about 50 angstroms and about 500 angstroms.

14. The reprogrammable metal-to-metal antifuse of claim 1, wherein said antifuse material layer comprises amorphous carbon doped with hydrogen in a concentration range of about 1 atomic percent to about 40 atomic percent.

15. The reprogrammable metal-to-metal antifuse of claim 14, wherein said antifuse material layer has a thickness of between about 50 angstroms and about 500 angstroms.

16. The reprogrammable metal-to-metal antifuse of claim 1, wherein said antifuse material layer is about 50 angstroms to 500 angstroms in thickness, and said lower adhesion-promoting layer and said upper adhesion-promoting layer each have a thickness of between about 2 angstroms and about 20 angstroms.

17. The reprogrammable metal-to-metal antifuse in claim 16, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer are from a material selected from the group comprising Si_xC_y and Si_xN_y.

18. The reprogrammable metal-to-metal antifuse of claim 17, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xC_y.

19. The reprogrammable metal-to-metal antifuse of claim 18, wherein a ratio of x to y in said Si_xC_y is in a range of about 1 +/- 0.4.

20. The reprogrammable metal-to-metal antifuse of claim 17, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xN_y.

21. The reprogrammable metal-to-metal antifuse of claim 20, wherein a ratio of x to y in said Si_xN_y is in a range of about .75 +/- 0.225.

22. The reprogrammable metal-to-metal antifuse of claim 17, wherein said amorphous carbon antifuse material layer is doped with hydrogen from about 1 atomic percent to about 40 atomic percent.

23. A reprogrammable metal-to-metal antifuse comprising:

a lower metal interconnect layer;

an inter-metal dielectric layer disposed over said lower metal interconnect layer, said inter-metal dielectric layer having a via formed therethrough and filled with a metal plug;

a lower Ti barrier layer disposed over said metal plug;

a lower adhesion-promoting layer disposed over said lower Ti barrier layer;

an antifuse material layer formed from amorphous carbon and disposed over said lower adhesion-promoting layer;

an upper adhesion-promoting layer disposed over said antifuse material layer;

an upper Ti barrier layer disposed over said upper adhesion-promoting layer; and

an upper metal interconnect layer disposed over said upper Ti barrier layer.

24. The reprogrammable metal-to-metal antifuse of claim 23, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer are comprised of a material selected from the group comprising Si_xC_y and Si_xN_y.

25. The reprogrammable metal-to-metal antifuse of claim 24, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xC_y.

26. The reprogrammable metal-to-metal antifuse of claim 25, wherein a ratio of x to y in said Si_xC_y is in a range of about 1 +/- 0.4.

27. The reprogrammable metal-to-metal antifuse of claim 24, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer comprise Si_xN_y.

28. The reprogrammable metal-to-metal antifuse of claim 27, wherein a ratio of x to y in said Si_xN_y is in a range of about .75 +/- 0.225.

29. The reprogrammable metal-to-metal antifuse of claim 23, wherein said antifuse material layer has a thickness of between about 50 angstroms and about 500 angstroms.

30. The reprogrammable metal-to-metal antifuse of claim 23, wherein said amorphous carbon antifuse material layer is doped with hydrogen in a concentration range of about 1 atomic percent to about 40 atomic percent.

31. The reprogrammable metal-to-metal antifuse of claim 30, wherein said amorphous carbon antifuse material layer has a thickness of between about 50 angstroms

and about 500 angstroms.

32. The reprogrammable metal-to-metal antifuse of claim 23, wherein said lower adhesion-promoting layer and said upper adhesion-promoting layer are comprised of a material selected from the group comprising Si_xC_y, Si_xN_y, $Si_xC_yN_z$, $Si_xO_yC_z$, and $Si_xO_yN_z$.

33. A reprogrammable metal-to-metal antifuse comprising:

a lower Ti barrier layer;

a lower Si_xC_y layer disposed over said lower Ti barrier layer;

an antifuse material layer comprised of amorphous carbon and disposed over said lower Si_xC_y layer;

an upper Si_xC_y layer disposed over said antifuse material layer; and

an upper Ti barrier layer.

34. A reprogrammable metal-to-metal antifuse comprising:

a lower Ti barrier layer;

a lower Si_xN_y layer disposed over said lower Ti barrier layer;

an antifuse material layer comprised of amorphous carbon and disposed over said lower Si_xN_y layer;

an upper Si_xN_y layer disposed over said antifuse material layer; and

an upper Ti barrier layer.

35. A method for fabricating a reprogrammable metal-to-metal antifuse, comprising:

planarizing an insulating layer and a tungsten plug;

forming a lower Ti barrier layer over said insulating layer and said tungsten plug;

forming a lower adhesion-promoting layer over said lower Ti barrier layer, said lower adhesion-promoting layer selected from the group comprising Si_xC_y and Si_xN_y;

forming an antifuse material layer over said lower adhesion-promoting layer, wherein said antifuse material layer is selected from the group comprising amorphous carbon, amorphous carbon doped with at least one of hydrogen and fluorine, and amorphous silicon carbide;

forming an upper adhesion-promoting layer over said antifuse material layer, said upper adhesion-promoting layer selected from the group comprising Si_xC_y and Si_xN_y;

forming an upper Ti barrier metal layer over said antifuse material layer;

forming an oxide or tungsten hardmask layer over said barrier metal layer;

forming a layer of photoresist over said hardmask layer;

defining said hardmask layer;

removing said photoresist;

defining a shape of a stack for said antifuse by etching said upper Ti barrier layer, said upper adhesion-promoting layer, said antifuse material layer, said lower adhesion-promoting layer, and said lower Ti barrier metal layer using said hardmask layer as a mask;

forming an insulating layer over said stack;

forming an aperture in said insulating layer;

forming a metal interconnect layer over said insulating layer and in said aperture;

forming a second masking layer over said metal interconnect layer; and

defining said metal interconnect layer.

36. The method of Claim 35, wherein said forming said antifuse material layer comprises forming said antifuse material layer to a thickness of from about 10 nm to about 80 nm.

37. The method of Claim 35, wherein said forming said Ti barrier metal layer comprises forming said Ti barrier metal layer to a thickness of from about 25 nm to about 200 nm.

38. The method of Claim 35, wherein said lower and upper adhesion-promoting layers are essentially monolayers.

39. The method of Claim 35, wherein said forming an antifuse material layer comprises depositing said antifuse layer from an acetylene source gas.

40. A method for programming and erasing a reprogrammable metal-to-metal antifuse, comprising:

programming said antifuse by applying a programming potential across said antifuse to cause a programming current to flow through said antifuse until its resistance substantially decreases; and

erasing said antifuse by applying an erasing potential across said antifuse, said erasing potential being lower in magnitude than said programming potential and causing an erase current to flow through said antifuse.

41. The method of claim 40 wherein applying a programming potential across said antifuse and applying an erasing potential across said antifuse both comprise applying a potential having a more negative value above said antifuse material layer.

42. The method of claim 40 wherein said programming current is in a range of between about 100μA to about 1mA.

43. The method of claim 40 wherein programming said antifuse also includes soaking said antifuse by passing a soak-current through said antifuse.

44. The method of claim 43 wherein said soak-current has a magnitude of about 5mA.

45. The method of claim 42 wherein said programming current is less than about 1mA and a ratio of said erase current to said programming current is about 10:1.

46. The method of claim 40 wherein:

said programming current is less than about 1mA;

programming said antifuse also includes soaking said antifuse by passing a soak-current having a magnitude of less than about 5mA; and

a ratio of said erase current to said soak current is about 3:1.

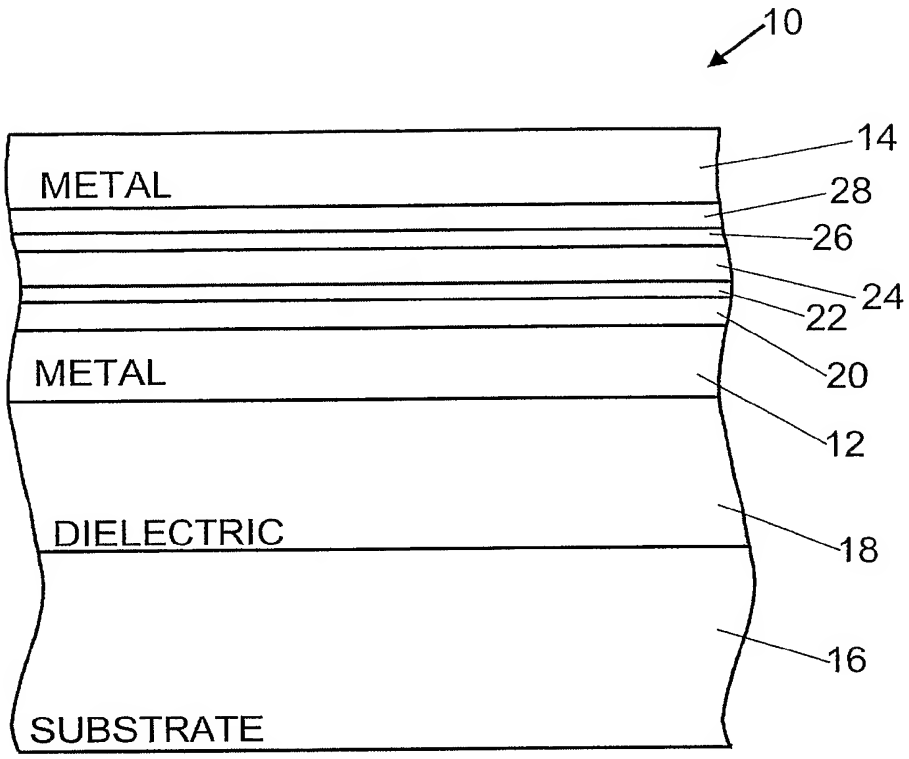

10
14
METAL
28
26
24
22
20
METAL
12
DIELECTRIC
18
16
SUBSTRATE

FIG. 1

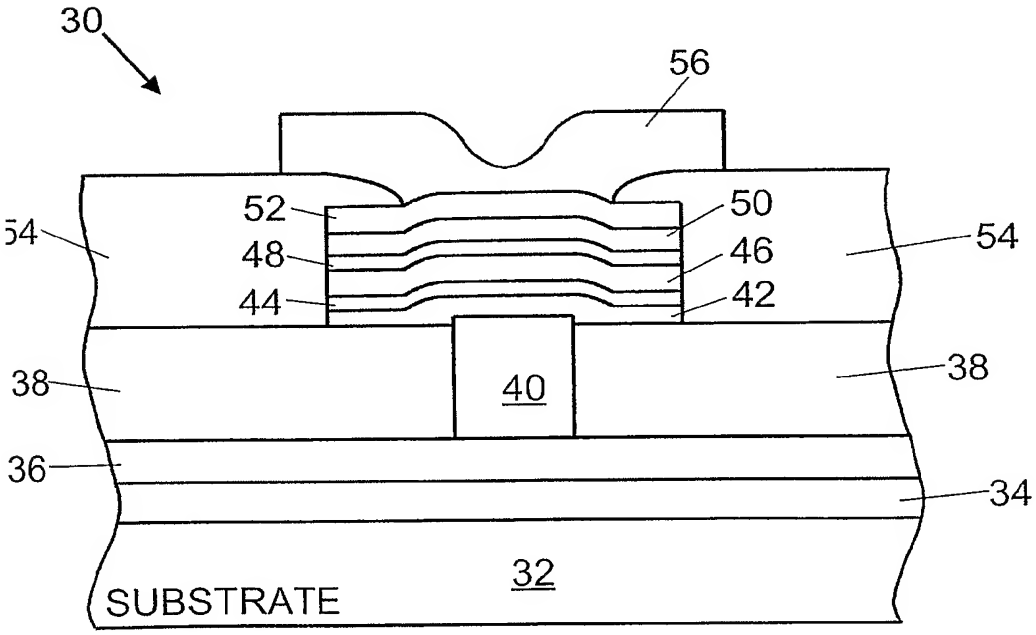

30
56
52
50
54
48
46
54
44
42
38
40
38
36
34
32
SUBSTRATE

FIG. 2A

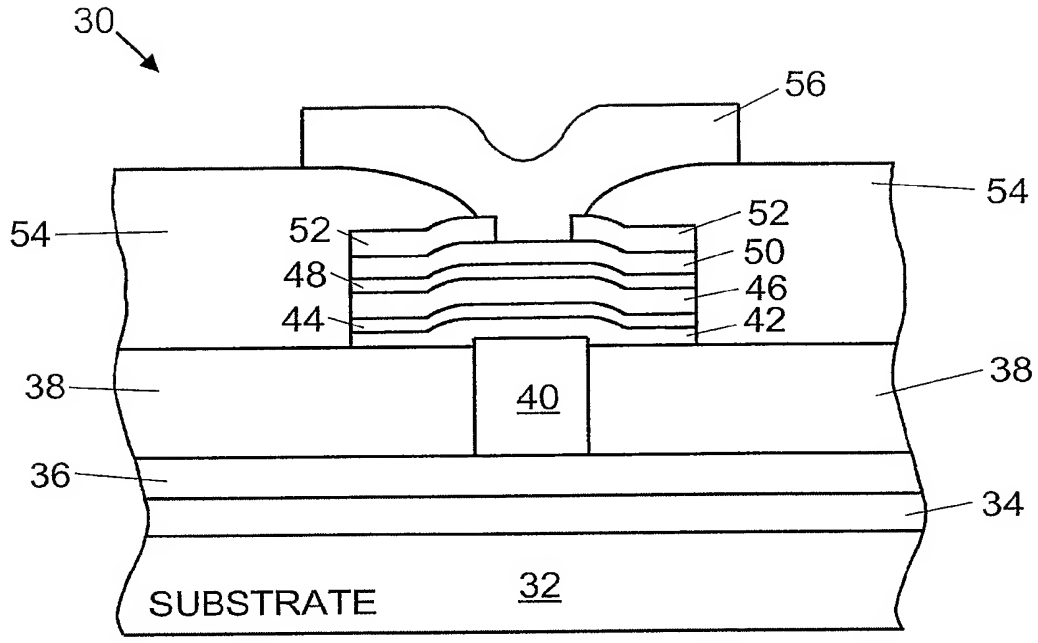

30
56
54
54
52
52
50
48
46
44
42
38
40
38
36
34
SUBSTRATE
32

FIG. 2B

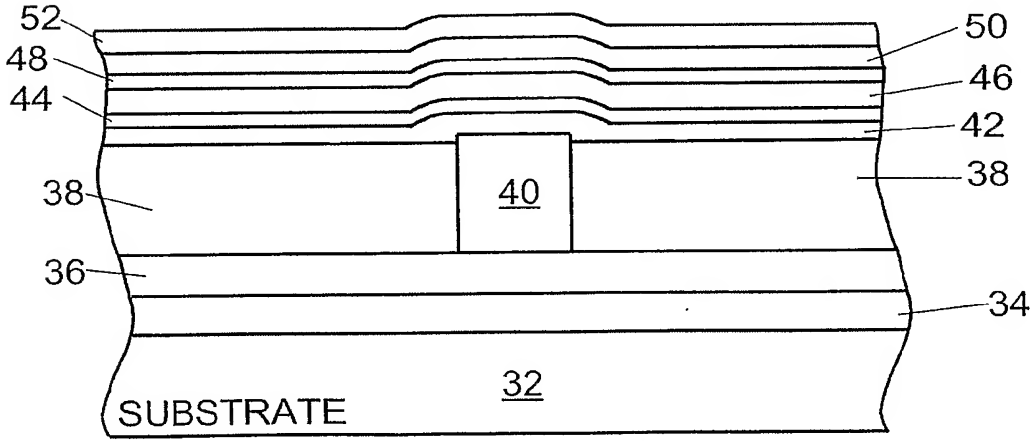

52
50
48
46
44
42
38
40
38
36
34
32
SUBSTRATE

FIG. 3A

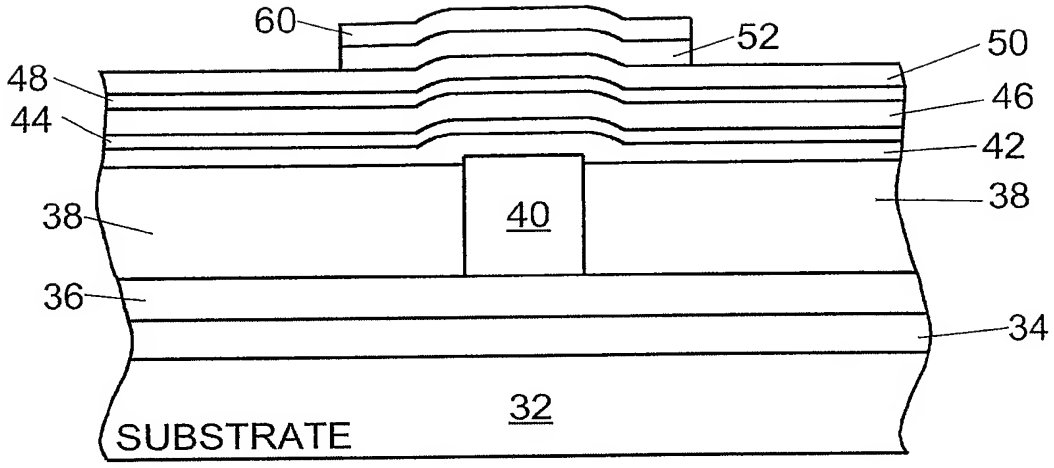

60
52
50
48
46
44
42
40
38
38
36
34
32
SUBSTRATE

FIG. 3B

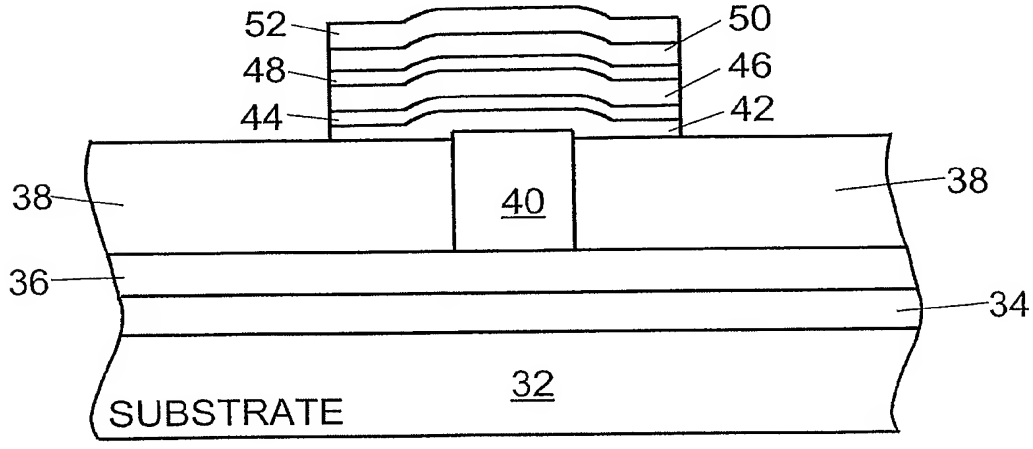

52
50
48
46
44
42
40
38
38
36
34
32
SUBSTRATE

FIG. 3C

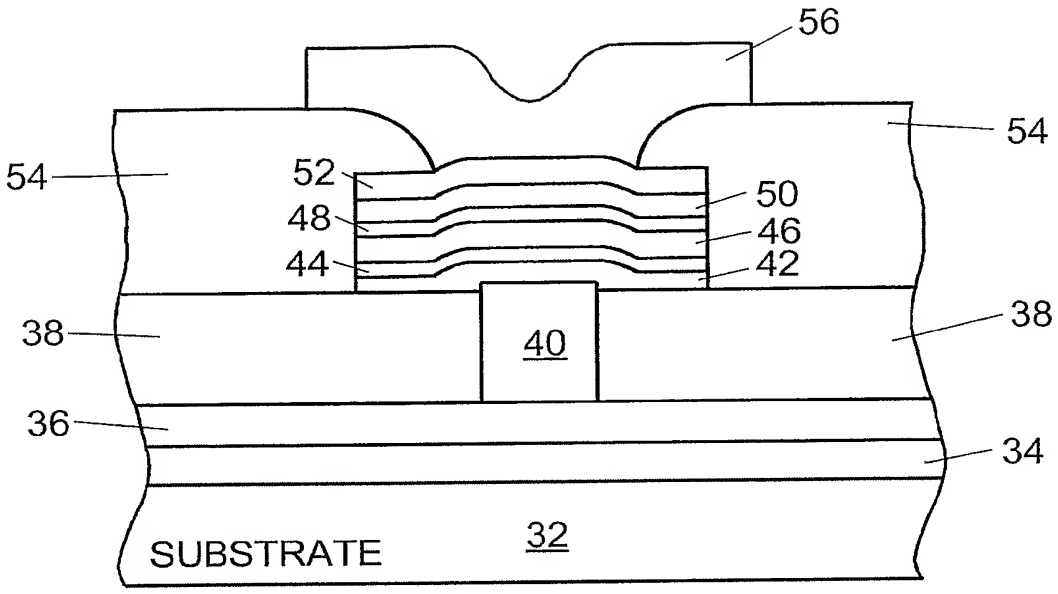

56
54
54
52
50
48
46
44
42
38
40
38
36
34
SUBSTRATE
32

FIG. 3D

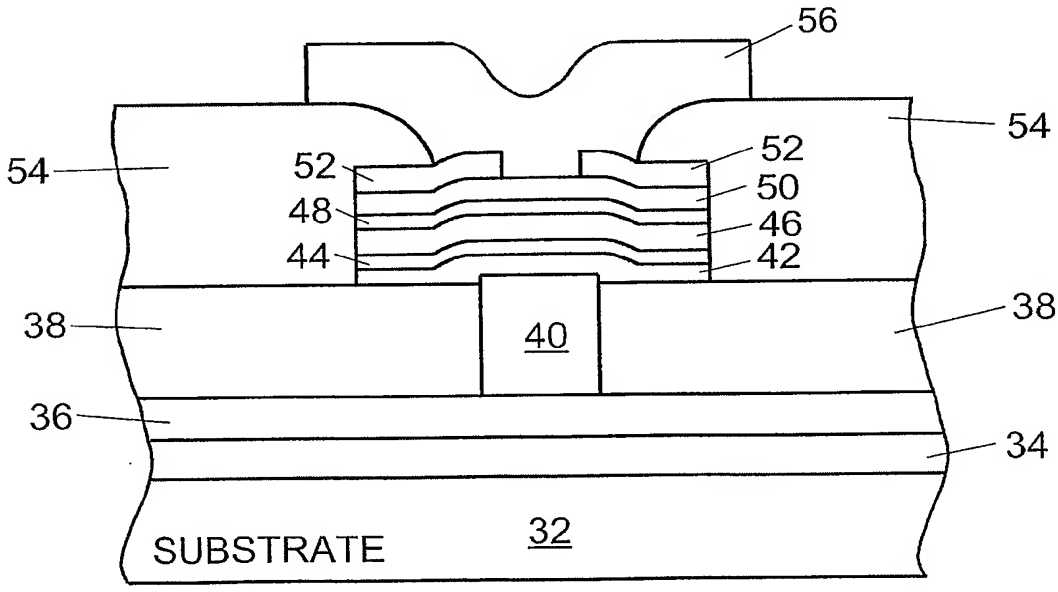

56
54
54
52
52
50
48
46
44
42
38
40
38
36
34
SUBSTRATE
32

FIG. 3E

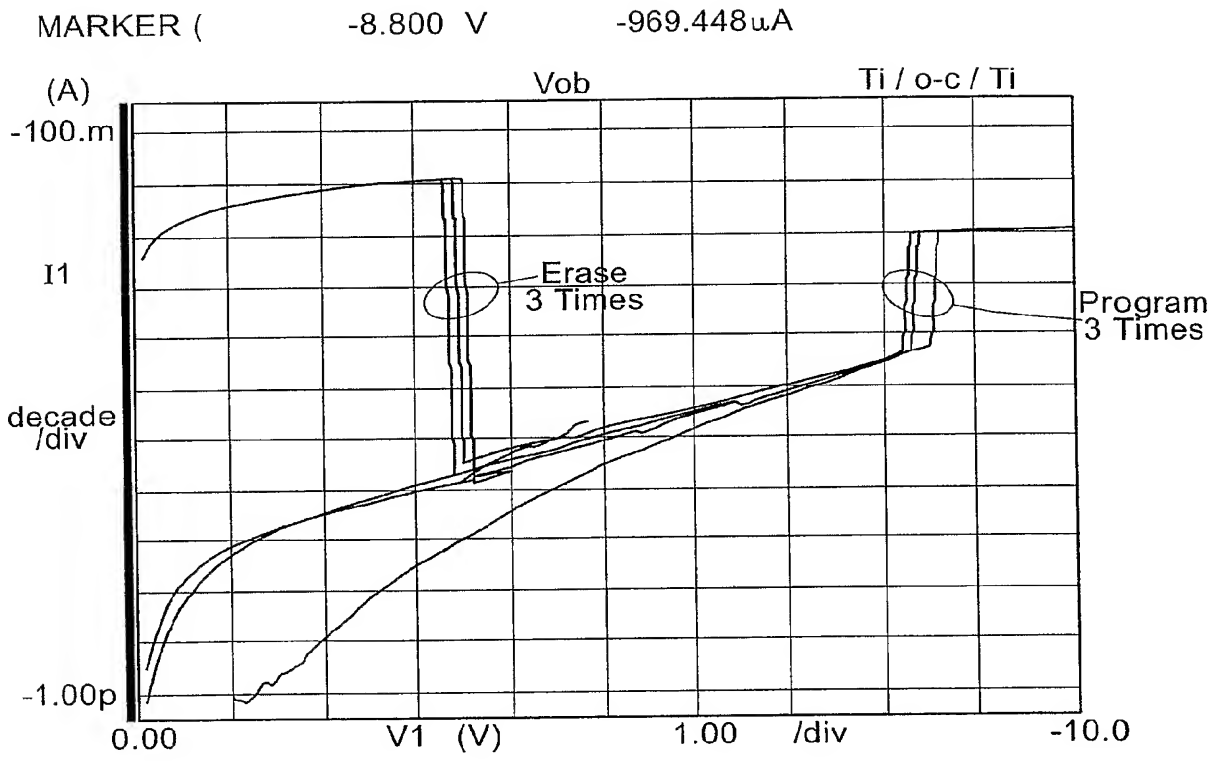

MARKER (-8.800 V -969.448uA
(A)
Vob
Ti / o-c / Ti
-100.m
I1
decade /div
-1.00p
Erase 3 Times
Program 3 Times
0.00
V1 (V)
1.00 /div
-10.0

FIG. 4

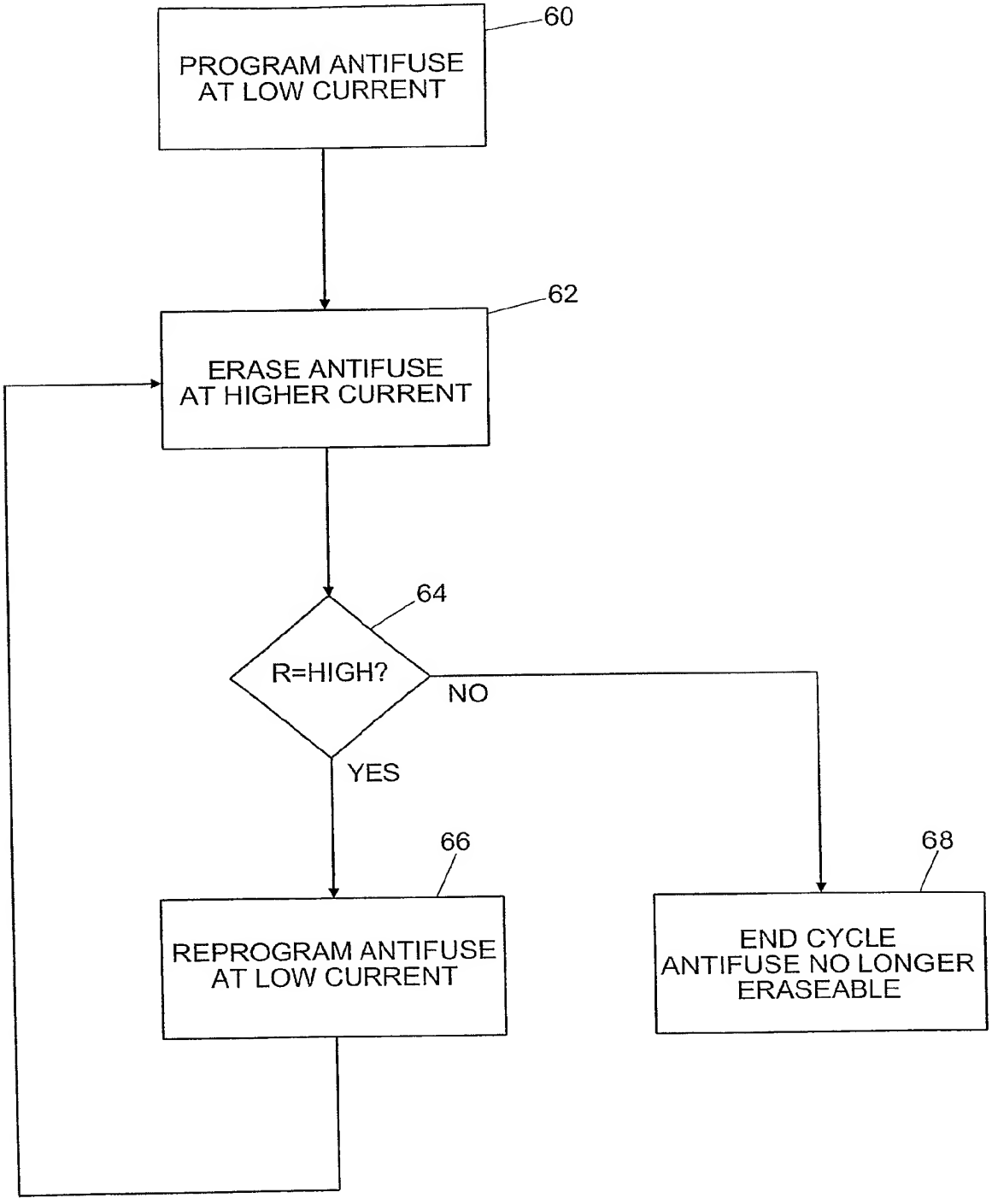

PROGRAM ANTIFUSE AT LOW CURRENT
60
ERASE ANTIFUSE AT HIGHER CURRENT
62
R=HIGH?
64
NO
YES
REPROGRAM ANTIFUSE AT LOW CURRENT
66
END CYCLE ANTIFUSE NO LONGER ERASEABLE
68

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/05749

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 31/0256, 31/0312, 29/00, 23/48

US CL : 257/76, 77, 529, 530, 751, 774

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/76, 77, 529, 530, 751, 774

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,181,096 (Forouhi) 19 January, 1993 (19.01.1993), figure 1, column 4, line 10 to column 5, line 66.	1-46
Y	Liu et al., A new metal to metal antifuse with amorphous carbon, IEEE Electron Device Letters, 1998, Vol. 19, No. 9, pages 317-319.	1-46
Y	US 5,789,764 (McCollum) 4 August 1998 (04.08.1998), figure 7C, column 9, lines 41-55	23-24, 27-32
Y	US 6,583,953 (Han et al.) 24 June, 2003 (24.06.2003), column 4, lines 21-24.	4-5, 9-10, 18-19, 25-26, 33

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

03 October 2005 (03.10.2005)

Date of mailing of the international search report

28 NOV 2005

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Facsimile No. (703) 305-3230

Authorized officer

Stephen Loke

Telephone No. 703-308-0956

Form PCT/ISA/210 (second sheet) (April 2005)